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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,436	03/25/2004	Min-Chih Hsuan	JCLA12013	9790

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J.C. Patents, Inc.
Suite 250
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01/10/2008

EXAMINER

ARORA, AJAY

ART UNIT	PAPER NUMBER
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2892

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/810,436

Applicant(s)

HSUAN ET AL.

Examiner

Ajay K. Arora

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 September 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 and 24 is/are pending in the application.
- 4a) Of the above claim(s) 2 and 9-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3-8 & 24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.


Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/ are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1, 3-7 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin (US 6,323,550), hereinafter Martin, in view of Meckes (US 7,061,098), hereinafter Meckes.

Regarding claim 1, Martin (refer to Figure 4) discloses a chip package, comprising:

a chip (10), having an active surface and a plurality of bond pads (16), said bond pads being on said active surface;

a rigid cover (50), on said active surface, said rigid cover exposing said plurality of bond pads (Col. 4, lines 16-21) above said active surface;

an adhesive layer (52), disposed between the chip and the rigid cover, and the rigid cover is adhered to the chip via the adhesive layer; and

a plurality of contacts (18/20) electrically connected to said plurality of bond pads (16), respectively.

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Martin does not specifically state that the chip package is "for disposing on a printed circuit board (PCB)" and that chip package contacts are "connected to the PCB".

However, it is well known in the art to connect the contacts of a chip package to a PCB.

It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Martin so that the chip package is "for disposing on a printed circuit board (PCB)" and that chip package contacts are connected to the PCB. The ordinary artisan would have been motivated to modify Martin for at least the purpose of connecting the chip package to other components of a specific circuit that may be mounted on a printed circuit board.

Further, Martin does not teach that the contacts are "conductive bumps" and that the rigid cover is "located between" the chip and the PCB. Meckes (refer to Figure 1) teaches a chip package with contacts, wherein the contacts are conductive bumps (14). Further, if the plurality of contacts (18/20) of Martin are replaced by the conductive bumps (14) of Meckes and when the chip package as modified above is disposed on a PCB using the conductive bumps to connect to the PCB in a conventional manner, it would follow that the rigid cover is located between the chip and the PCB. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Martin so that the contacts are conductive bumps and mount the package to a PCB using the conductive bumps such that the rigid cover is located between the chip and the PCB. The ordinary artisan would have been motivated to modify Martin for at least the purpose of providing an interconnect type that can provide a greater

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interconnect density (for example, compared to wirebonds of Martin) and more compact overall package.

Regarding claim 3, Martin (refer to Figure 4) teaches that said rigid cover (50) is adhered to said active surface.

Regarding claim 4, Martin (refer to Figure 4) teaches said rigid cover (50) having a periphery adhered to said active surface.

Regarding claim 5, Martin (refer to Figure 4) teaches that the material of said rigid cover (50) includes a conducting material (Col. 4, lines 11-13 and Col. 5, 17-19).

Regarding claim 6, Martin (refer to Figure 4) as modified above for claim 1 teaches substantially the claimed structure including the chip package with said plurality of contacts that are disposed on said plurality of bond pads respectively, but does not teach that "the heights of said contacts relative to said active surface are larger than the height of said rigid cover relative to said active surface". Meckes (refer to Figure 1) teaches a chip package with a cover (9) on said an active surface (5) of the chip and a plurality of bond pads (6) and a plurality of contacts (14) on said plurality of bond pads respectively, wherein the heights of said contacts (14) relative to said active surface (5) are larger than the height of said cover (9) relative to said active surface. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the

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invention of Martin so that the heights of said contacts relative to said active surface are larger than the height of said rigid cover relative to said active surface. The ordinary artisan would have been motivated to modify Martin for at least the purpose of utilizing flip chip interconnections to connect the chip package to a substrate (e.g. a printed circuit board), wherein the height of the said contacts provides a clearance between the substrate and the chip surface to accommodate typical processing like cleaning after soldering.

Regarding claim 7, Martin (refer to Figure 4) teaches that the plurality of bond pads (16) is disposed on the circumference of said active surface. Note that the claim does not require the said active surface to be circular. Hence, the word "circumference" is being interpreted as the peripheral region of the said active surface.

Regarding claim 24, Martin as modified above teaches substantially the claimed structure including bond pads (16) disposed on said active surface as an array and said rigid cover (50) is located above said active surface, but does not teach that the rigid cover has "a plurality of openings corresponding to said bond pads and exposing said bond pads respectively". Instead, Martin teaches that the rigid cover exposes said bond pads by not extending the rigid cover to the bond pads. Meckes (refer to Figure 1) teaches a chip package with bond pads (6) disposed as an array and a cover (8/9), wherein the cover has a plurality of openings corresponding to said bond pads and exposing said bond pads respectively. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Martin so that the

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rigid cover has a plurality of openings corresponding to said bond pads and exposing said bond pads respectively. The ordinary artisan would have been motivated to modify Martin for at least the purpose of extending the rigid cover to protect a larger surface of the chip including the surface in the vicinity of the bond pads while also providing a means (i.e. openings in the rigid cover) for forming chip interconnects for connecting the chip to external components.

It is to be noted that "an array" is a generic term and is hence not required to be an array of any specific size. Thus, even a single column array is also an array.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin in view of Meckes, and further in view of Nishiguchi (JP 04024928), hereinafter Nishiguchi.

Regarding claim 8, Martin as modified above teaches substantially the claimed structure but does not specifically state that the active surface area "is a rectangle" and that the said plurality of bond pads are "disposed on one side of said rectangle".

Nishiguchi teaches a chip with a rectangular active surface area (see English abstract, 1st sentence under the heading "Constituion"). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Martin so that the said active surface is a rectangle and that the said plurality of bond pads are disposed on one side of said rectangle. The ordinary artisan would have been

motivated to modify Martin for at least the purpose of symmetrical arrangement of bond pads that can improve recognition of features by pattern recognition equipment.

Response to Arguments

Applicant's arguments filed 09/17/2007 with respect to the amendment to claim 1 and new claim 24 have been considered but are moot in view of the new ground(s) of rejection.

However, some arguments that are not covered by the rejection will be addressed here.

On page 6, applicant argues that "Martin fails to teach or suggest that the leadframe style package can be changed to a flip-chip style package by using bumps to connect the chip to the carrier". In response to applicant's above argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it is well known in the art that interconnection of a chip to external components, including PCBs, may be accomplished by a variety of interconnection schemes, including leaded interconnects (as taught by Martin) or leadless interconnects (like flip-chip style

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interconnects taught by Meckes). Therefore, simply using a different (but known) interconnection scheme is in the knowledge generally available to one of ordinary skill in the art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.


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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AKA

Date: January 3, 2008


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